Please amend Page 10, lines 12-22, as follows:

The imaging circuit may further comprise means for comparing signals from pixels of the detectors with an upper or lower limit of a dynamic range of the reading circuit, means for generating variation data of the detectors based on the result of the comparison, and means for manipulating a most significant bit (MSB) of each of the variation data of the detectors to determine a value of the MSB based on the result of the comparison, and successively manipulating bits of the variation data of the detectors to determine values of the bits up to a least significant bit thereof.

Please amend Page 15, lines 22-26 continuing to page 16, lines 1-16, as follows:

The emitter sizes (m) of the NPN transistors 116 are different for the following reasons: The relationship between the base current I_B and the base-to-emitter voltage V_{BE} is expressed by

$$I_B = mIB_0Exp[qV_{BE}/kT]$$

where IB_0 represents a reverse leakage current, q a unit charge, k the Boltzmann's constant, and T the absolute temperature. Since the base current is expressed by $I_B = I_c/\beta$ where β is the current amplification factor, if the collector current changed with the emitter size m being constant, the base-to-emitter voltage V_{BE} would also change. Because the same voltage V_{bl} is applied to the bases of the transistors 116, if the base-to-emitter voltage V_{BE} were different from state to state, the currents in the respective stages would not be established as described above. By changing the emitter size m depending on the current, the base-to-emitter voltages V_{BE} in the respective stages become equal to each other, and currents in the respective stages

Q3 Ent

can be established as described above.

Please amend Page 17, lines 14-26 continuing to page 18, lines 1-5, as follows:

Q4

The total noise can be reduced by increasing the emitter resistance. If the emitter resistance is increased to 1 KΩ or more, the total noise starts to decrease. If the emitter resistance is 5 KΩ or higher, the total noise is about 3 dB lower than if the emitter resistance is 1 KΩ or less. The value of 3 dB is a limit value at which the human eye can recognize the improved total noise. When the collector current is 10 μA, then the voltage across the emitter resistance is 5 V or lower if the emitter resistance is 500 kΩ or less, and can be handled by an ordinary BiCMOS circuit. If the emitter resistance is 100 kΩ or less, then the voltage across the emitter resistance is 1 V or less, providing a margin to the dynamic range of the circuit. Therefore, the emitter resistance should range from 1 kΩ to 500 kΩ, preferably from 5 kΩ to 100 kΩ.

Please amend page 18, lines 18-26 continuing to page 19, lines 1-10, as follows:

Q5

In order to reduce temperature drifts of the imaging device, it is necessary to reduce the temperature dependency of the currents I_0, 2 I_0, 4 I_0, . . . of the FPN correction regulated constant-current source 113. To meet this requirement, a base voltage V_{b3} serving as a basis for the currents I_0, 2 I_0, 4 I_0, . . . is designed so as to be less temperature dependent. The base voltage V_{b3} may be generated within or supplied from outside of the FPN correction regulated constant-current source 113. For reduced temperature dependency, however, it is preferable to use a regulated constant-voltage source having a very small temperature dependency

property such as a band gap reference or the like for generating the base voltage V_{b3}. In infrared imaging device applications, such a regulated constant-voltage source may be formed on a chip for a constant temperature because the chip may be or kept at a normal temperature by a Peltier device.

Please amend page 30, lines 8-20 as follows:

Fig. 8 shows a process of generating the FPN correction data. It is assumed that the number of bits of the FPM correction data is 3. The process shown in Fig. 8 comprises a step 601 of clearing data of all addresses of the FPN memory 513, a step 602 of changing bit positions from most significant bit (MSB) to least significant bit (LSB), a step 603 of setting a bit b of all addresses of the FPN memory 513 to 1, an instruction step 604 for changing V addresses, an instruction step 605 of changing H addresses, a step 606 of making a conditional jump based on the decision made by the comparator 511, and a step 607 of resetting a bit b of a certain address of the FPN memory 513 to 0.

IN THE CLAIMS:

Please amend claims 1, 11-14, and 20-22 to read as follows:

1. (Amended) An imaging device comprising:

a plurality of detectors for converting an electromagnetic radiation into electric signals;

a plurality of read circuits, each connected to at least one of said detectors, and including a first regulated constant-current source for supplying a constant bias current to said